

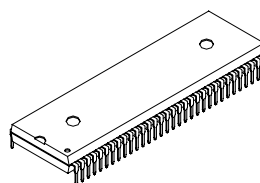
**CMOS 8-bit Single Chip Microcomputer****Description**

The CXP851P16 are highly integrated microcomputers composed of a 8-bit CPU, PROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, vector interrupt, on-screen display function, I<sup>2</sup>C bus interface, PWM generator, remote control receiver, HSYNC counter, power supply frequency counter, and watchdog timer.

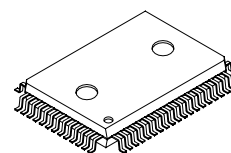
Also this IC provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful microcomputers.

The CXP851P16 is the on-chip PROM version of the CXP85116 with on-chip mask ROM, providing the function of being able to write directly into the program. Furthermore, because of the OSD character ROM can also be written directly into, it is suitable for evaluation use during system development and for small quantity production.

64 pin SDIP (Plastic)



64 pin QFP (Plastic)

**Structure**

Silicon gate CMOS IC

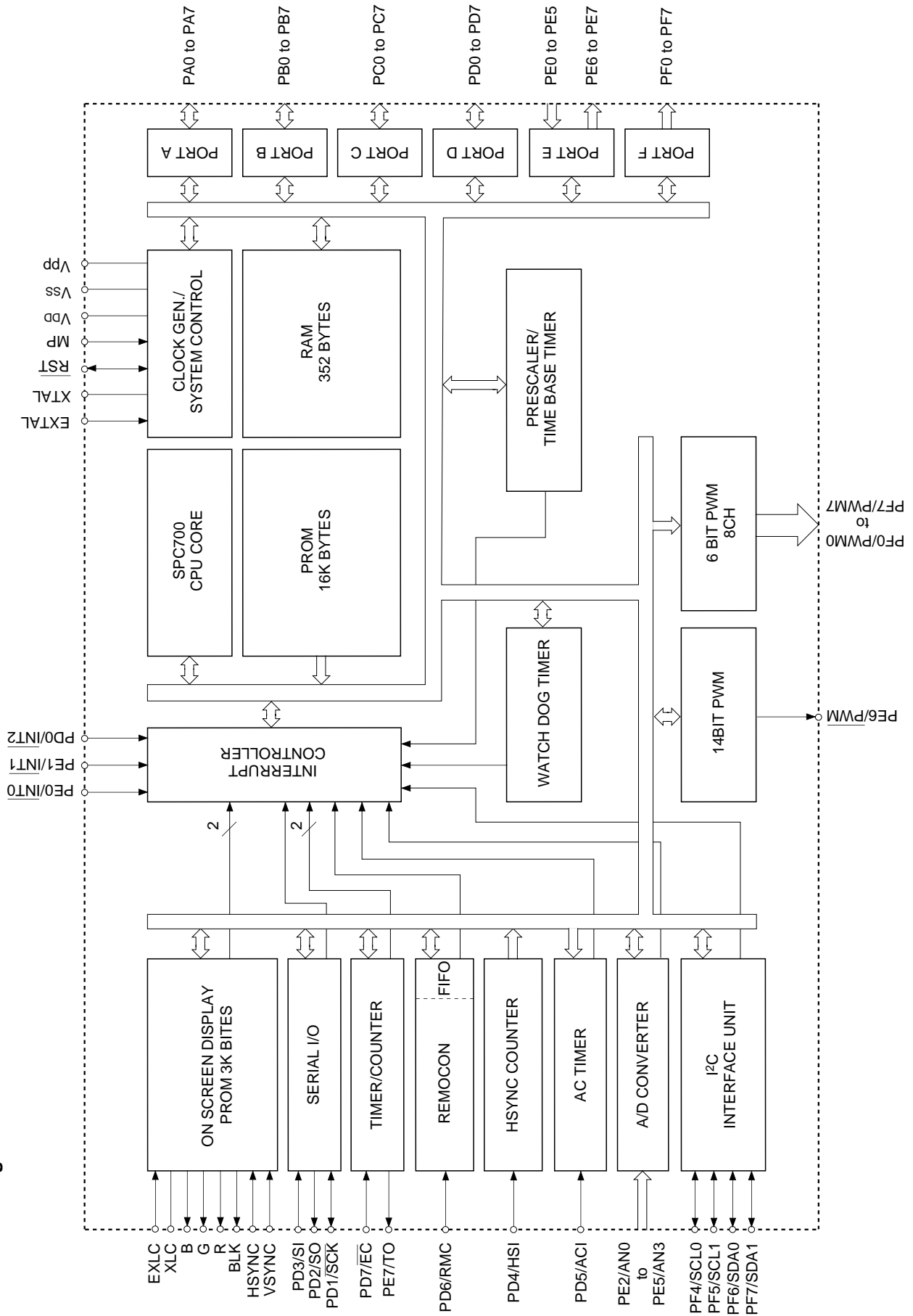
**Features**

- A wide instruction set (213 instructions) which cover various types of data.
  - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle                      During operation 1 $\mu$ s/4MHz
- Incorporated PROM capacity                      16K bytes (For program)  
3K bytes (For OSD)
- Incorporated RAM capacity                        352 bytes
- Peripheral functions
  - On-screen display function                    12  $\times$  16 dots, 128 types  
4 lines of 21 characters (5 or more lines possible)  
double scanning mode supported includes jitter elimination circuit
  - I<sup>2</sup>C bus interface
  - PWM output                                        14-bits, 1 channel  
6-bits, 8 channels
  - Remote control receiving circuit            8-bit pulse measuring counter, 6-stage FIFO
  - A/D converter                                     4-bit, 4-channel, successive approximation method  
(conversion time of 40 $\mu$ s/4MHz)
  - HSYNC counter
  - Power supply frequency counter
  - Watchdog timer
  - 8-bit synchronized serial I/O
  - 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- Interruption                                         14 factors, 14 vectors, multiple interrupt possible
- Standby mode                                       SLEEP/STOP
- Package     64-pin plastic SDIP/QFP

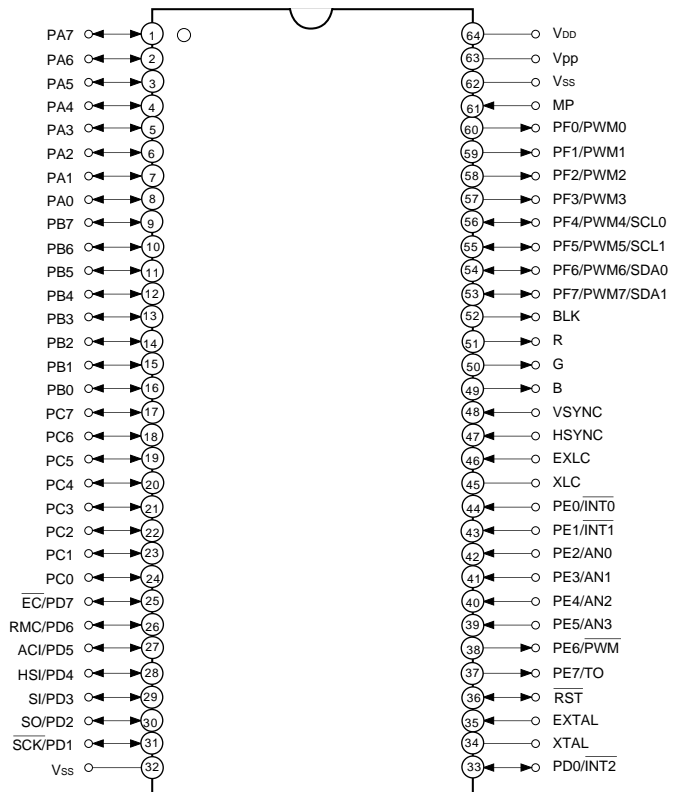
Purchase of Sony's I<sup>2</sup>C components conveys a licence under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

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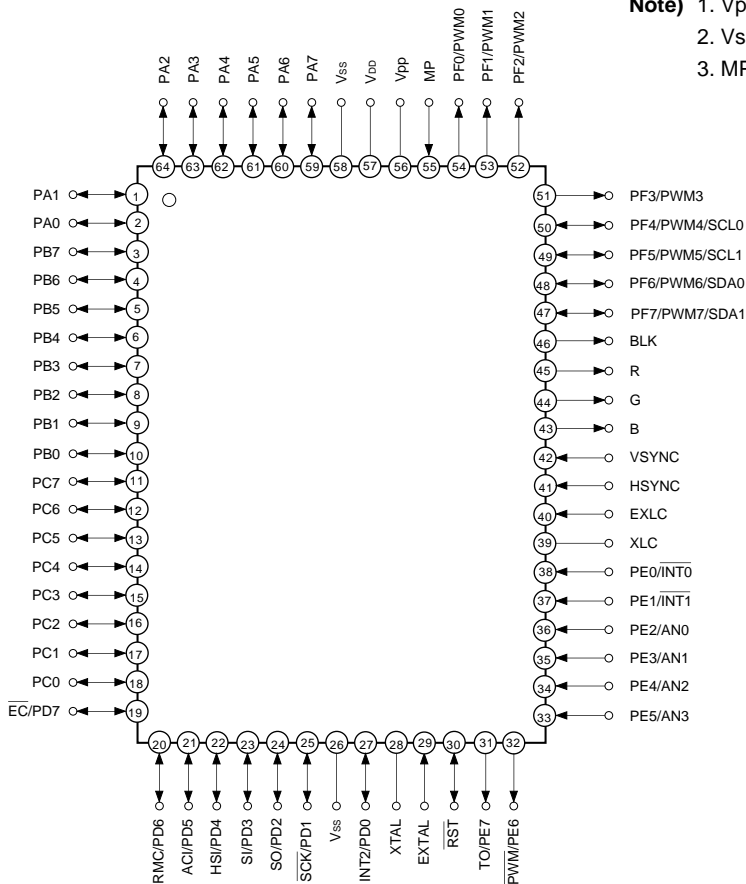
Block Diagram



Pin Configuration (Top View)



- Note)**
1. Vpp (Pin 63) is always connected to VDD.
  2. Vss (Pins 32 and 62) are both connected to GND.
  3. MP (Pin 61) is always connected to GND.



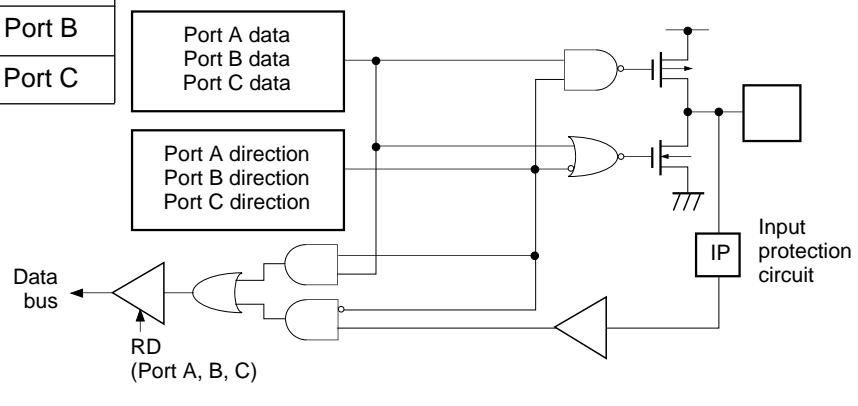
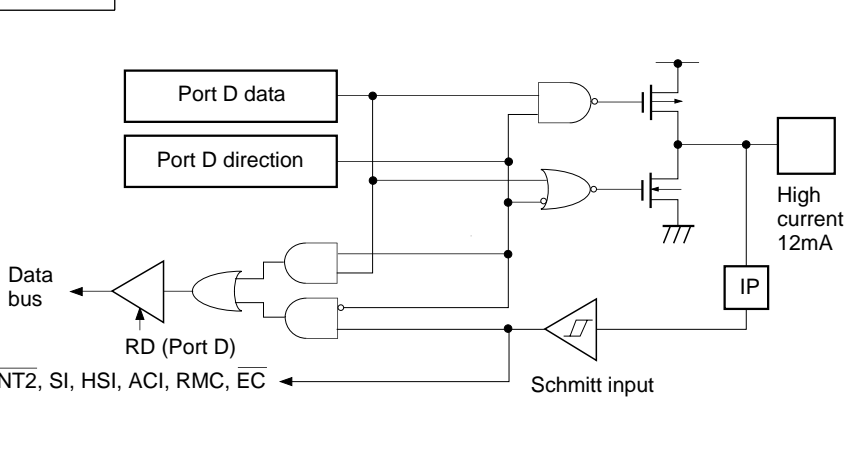
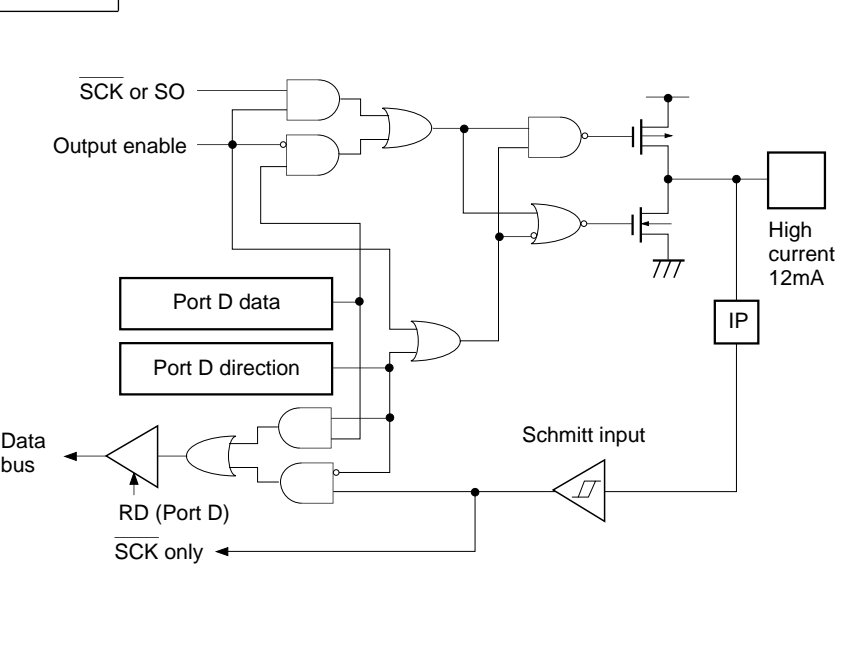
- Note)**
1. Vpp (Pin 56) is always connected to VDD.
  2. Vss (Pins 26 and 58) are both connected to GND.
  3. MP (Pin 55) is always connected to GND.

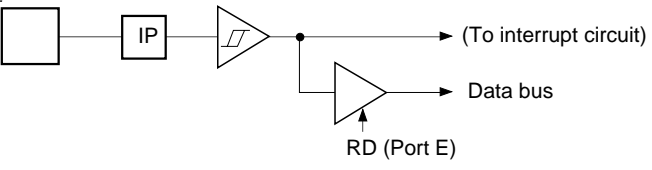
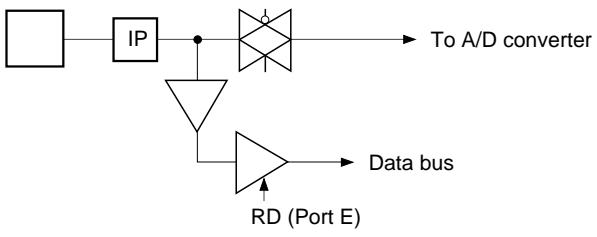
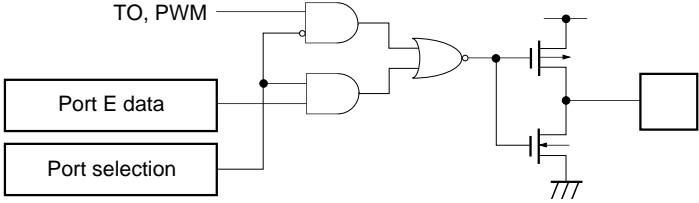
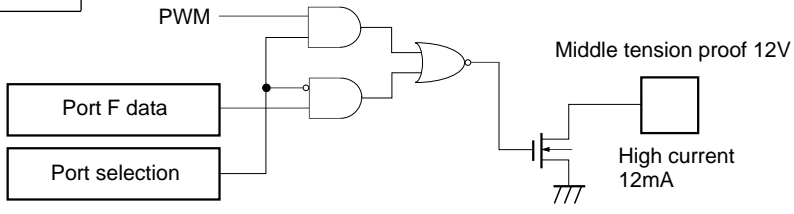
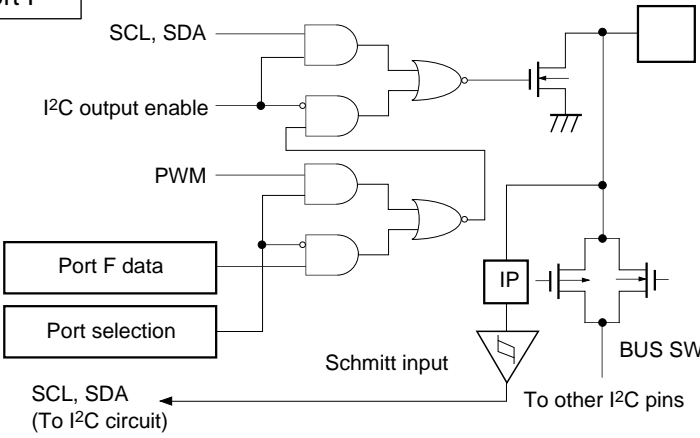
Pin Description

Symbol	I/O	Description	
PA0 to PA7	I/O	(Port A) Single bit selectable 8-bit port. (8 lines)	
PB0 to PB7	I/O	(Port B) Single bit selectable 8-bit port. (8 lines)	
PC0 to PC7	I/O	(Port C) Single bit selectable 8-bit port. (8 lines)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) Single bit selectable 8-bit port. 12mA sink current drive possible. (8 lines)	Input pin for external interrupt request. Active on falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock pin.
PD2/ $\overline{\text{SO}}$	I/O/Output		Serial data output pin.
PD3/ $\overline{\text{SI}}$	I/O/Input		Serial data input pin.
PD4/ $\overline{\text{HSI}}$	I/O/Input		HSYNC counter input pin.
PD5/ $\overline{\text{ACI}}$	I/O/Input		Power supply frequency counter input pin.
PD6/ $\overline{\text{RMC}}$	I/O/Input		Remote control receiver circuit input pin.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event timer/counter input pin.
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port, lower 6 bits for input, upper 2 bits for output. (8 lines)	Input pin for external interrupt request. Active on falling edge. (2 lines)
PE2/ $\overline{\text{AN0}}$ to PE5/ $\overline{\text{AN3}}$	Input/Input		Analog input pin for A/D converter. (4 lines)
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)
PE7/ $\overline{\text{TO}}$	Output/Output		Square wave output for timer 1. (50% duty cycle)
PF0/ $\overline{\text{PWM0}}$ to PF3/ $\overline{\text{PWM3}}$	Output/Output	(Port F) 8-bit output port with large current (12mA) N-ch open drain output. Lower 4 bits middle voltage tolerance (12V), upper 4 bits 5V suppression. (8 lines)	6-bit PWM output pin. (8 lines)
PF4/ $\overline{\text{PWM4}}$ / SCL0 PF5/ $\overline{\text{PWM5}}$ / SCL1	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer clock input/output pin.
PF6/ $\overline{\text{PWM6}}$ / SDA0 PF7/ $\overline{\text{PWM7}}$ / SDA1	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer data input/output pin.
R, G, B, BLK	Output	CRT display 4-bit output pin.	
HSYNC	Input	CRT display horizontal synchronization signal input pin.	
VSYNC	Input	CRT display vertical synchronization signal input pin.	

Symbol	I/O	Description
EXLC	Input	CRT display clock oscillator input/output pin. Oscillator frequency is determined by external L, C circuit.
XLC	Output	
EXTAL	Input	System clock oscillator crystal connection pin. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	"L" level active system reset. This pin also acts as an input/output pin during power up. While internal power-on reset function is taking place a "L" level is output. (Mask option)
MP	Input	Microprocessor mode input pin. Must be connected to GND.
V <sub>DD</sub>		Positive power supply pin.
V <sub>pp</sub>		Positive power supply pin for on-chip PROM writing. Please connect to V <sub>DD</sub> for normal operation.
V <sub>ss</sub>		GND. Both V <sub>ss</sub> pins should be connected to common GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0 to PA7 PB0 to PB7 PC0 to PC7</p> <p>24 pins</p>	<p>Port A Port B Port C</p>  <p>Port A data Port B data Port C data</p> <p>Port A direction Port B direction Port C direction</p> <p>Data bus</p> <p>RD (Port A, B, C)</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PD0/<math>\overline{\text{INT2}}</math> PD3/SI PD4/HSI PD5/ACI</p> <p>PD6/RMC</p> <p>PD7/<math>\overline{\text{EC}}</math></p> <p>6 pins</p>	<p>Port D</p>  <p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p>Schmitt input</p> <p>High current 12mA</p> <p><math>\overline{\text{INT2}}</math>, SI, HSI, ACI, RMC, <math>\overline{\text{EC}}</math></p>	<p>Hi-Z</p>
<p>PD1/<math>\overline{\text{SCK}}</math> PD2/SO</p> <p>2 pins</p>	<p>Port D</p>  <p><math>\overline{\text{SCK}}</math> or SO</p> <p>Output enable</p> <p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p>SCK only</p> <p>Schmitt input</p> <p>High current 12mA</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/<math>\overline{\text{INT0}}</math> PE1/<math>\overline{\text{INT1}}</math></p> <p>2 pins</p>	<p>Port E</p> <p>Schmitt input</p>  <p>(To interrupt circuit)</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE2/<math>\overline{\text{AN0}}</math> to PE5/<math>\overline{\text{AN3}}</math></p> <p>4 pins</p>	<p>Port E</p> <p>Input multiplexer</p>  <p>To A/D converter</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE6/<math>\overline{\text{PWM}}</math> PE7/<math>\overline{\text{TO}}</math></p> <p>2 pins</p>	<p>Port E</p> <p>TO, <math>\overline{\text{PWM}}</math></p> <p>Port E data</p> <p>Port selection</p>  <p>H level</p>	<p>H level</p>
<p>PF0/<math>\overline{\text{PWM0}}</math> to PF3/<math>\overline{\text{PWM3}}</math></p> <p>4 pins</p>	<p>Port F</p> <p>PWM</p> <p>Port F data</p> <p>Port selection</p> <p>Middle tension proof 12V</p> <p>High current 12mA</p>  <p>Hi-Z</p>	<p>Hi-Z</p>
<p>PF4/<math>\overline{\text{PWM4}}</math>/ SCL0 PF5/<math>\overline{\text{PWM5}}</math>/ SCL1 PF6/<math>\overline{\text{PWM6}}</math>/ SDA0 PF7/<math>\overline{\text{PWM7}}</math>/ SDA1</p> <p>4 pins</p>	<p>Port F</p> <p>SCL, SDA</p> <p>I<sup>2</sup>C output enable</p> <p>PWM</p> <p>Port F data</p> <p>Port selection</p> <p>Schmitt input</p> <p>BUS SW</p> <p>To other I<sup>2</sup>C pins</p> <p>SCL, SDA (To I<sup>2</sup>C circuit)</p>  <p>Hi-Z</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>BLK R G B</p> <p>4 pins</p>	<p>To output polarity register Writing data to port register brings output from high impedance to active</p>	<p>Hi-Z</p>
<p>HSYNC VSYNC</p> <p>2 pins</p>		<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>		<p>Oscillation halted</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	<ul style="list-style-type: none"> <li>• Diagram indicates equivalent circuit during oscillation</li> <li>• Feedback resistor is disconnected during STOP</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>		<p>L level</p>
<p>MP</p> <p>1 pin</p>		<p>Hi-Z</p>



## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V <sub>IN</sub>	-0.3 to +7.0*1	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0*1	V	
Medium voltage tolerance output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Excludes large current output
	I <sub>OLC</sub>	20	mA	Large current output*2
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>d</sub>	1000	mW	SDIP
		600	mW	QFP

\*1) V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*2) The high current operation transistors are the N-ch transistors of the PD and PF0 to PF3 ports.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operation Conditions

(V<sub>SS</sub> = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed range for low speed data *1
		2.5	5.5	V	Guaranteed data hold operation range during stop
	V <sub>pp</sub>	V <sub>pp</sub> = V <sub>DD</sub>		V	*5
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	I <sup>2</sup> C Schmitt input included *2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS Schmitt input *3
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin *4
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	I <sup>2</sup> C Schmitt input included *2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS Schmitt input *3
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin *4
Operating temperature	T <sub>opr</sub>	-10	+75	°C	

\*1) Rating for 1/16 frequency mode and sleep mode.

\*2) Normal input port (All pins of PA, PB, PC, PE2 to PE5), PF4 to PF7, and MP pins.

\*3) Includes PD0/ $\overline{\text{INT2}}$ , PD1/ $\overline{\text{SCK}}$ , PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/ $\overline{\text{EC}}$ , PE0/ $\overline{\text{INT0}}$ , PE1/ $\overline{\text{INT1}}$ , HSYNC, VSYNC,  $\overline{\text{RST}}$  pins.

\*4) It specifies only when the external clock is input.

\*5) V<sub>pp</sub> and V<sub>DD</sub> should be set to a same voltage.

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PD, PE6, PE7, R, G, B, BLK	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V
Low level output voltage	V <sub>OL</sub>	PA to PD, PE6, PE7, R, G, B, BLK, PF0 to PF3, $\overline{\text{RST}}$	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA			0.6	V
		PD, PF0 to PF3	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.0mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 4.0mA			0.6	V
Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5		40	μA
	I <sub>IHL</sub>		V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-0.5		-40	μA
	I <sub>ILR</sub>	$\overline{\text{RST}}$	V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-1.5		-400	μA
Input/output leak current	I <sub>Iz</sub>	PA to PE, HSYNC, VSYNC, R, G, B, BLK, MP	V <sub>DD</sub> = 5.5V V <sub>I</sub> = 0, 5.5V			±10	μA
Open drain output leak current (N-ch Tr off case)	I <sub>LOH</sub>	PF0 to PF3	V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 12.0V			50	μA
		PF4 to PF7	V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 5.5V			10	μA
I <sup>2</sup> C bus switch connection impedance (output Tr off case)	R <sub>BS</sub>	SCL0: SCL1 SDA0: SDA1	V <sub>DD</sub> = 4.5V V <sub>SCL0</sub> = V <sub>SCL1</sub> = 2.25V V <sub>SDA0</sub> = V <sub>SDA1</sub> = 2.25V			120	Ω
Supply current	I <sub>DD</sub>	V <sub>DD</sub> *	Operating mode* (1/2 clock rate) 4MHz crystal oscillator (C <sub>1</sub> = C <sub>2</sub> = 22pF) All output pins open		10	25	mA
	I <sub>DDSL</sub>				0.7	3	mA
	I <sub>DDST</sub>					30	μA
Input capacitance	C <sub>IN</sub>	Pins other than V <sub>DD</sub> and V <sub>SS</sub>	1MHz clock 0V other than the measure pins		10	20	pF

\* Rating applies only if OSD oscillator is halted.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	3.5	4.5	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive	100		ns
System clock rise and fall times	t <sub>CR</sub> , t <sub>CF</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive		200	ns
Event counter input clock pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{EC}$	Fig. 3	t <sub>sys</sub> + 50*		ns
Event counter input clock rise and fall times	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{EC}$	Fig. 3		20	ms

\* t<sub>sys</sub> indicates three values according to the contents of the clock control register (address: 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

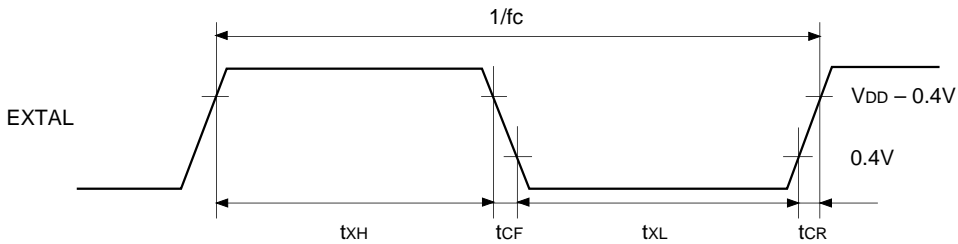


Fig. 2. Clock applied condition

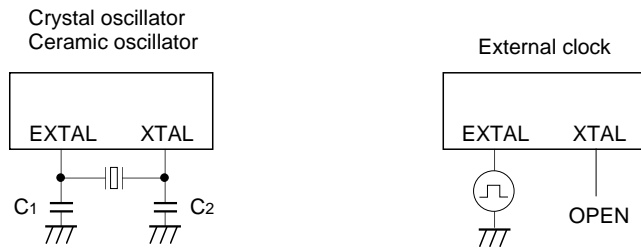
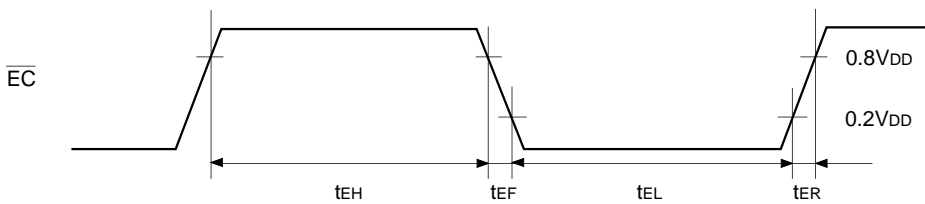


Fig. 3. Event count clock timing



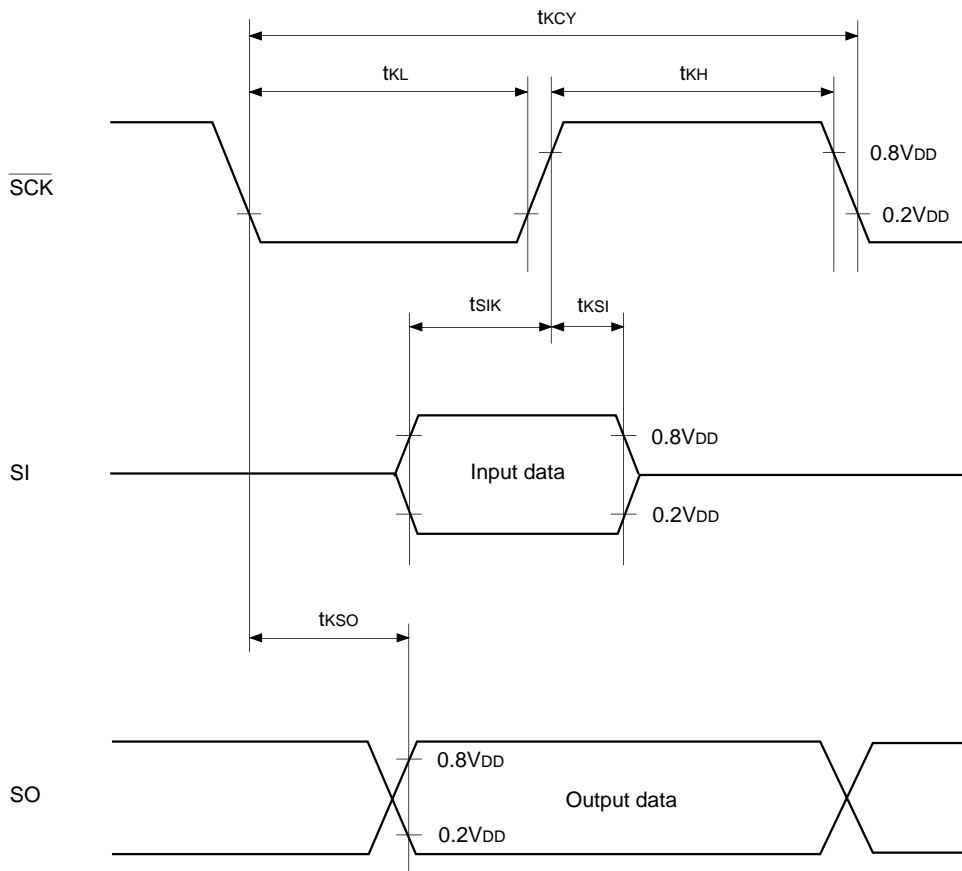
(2) Serial transfer

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ high and low level widths	$t_{\text{KH}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
	$t_{\text{KL}}$		$\overline{\text{SCK}}$ output mode	4000/fc - 50		ns
SI input set up time (against $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (against $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing

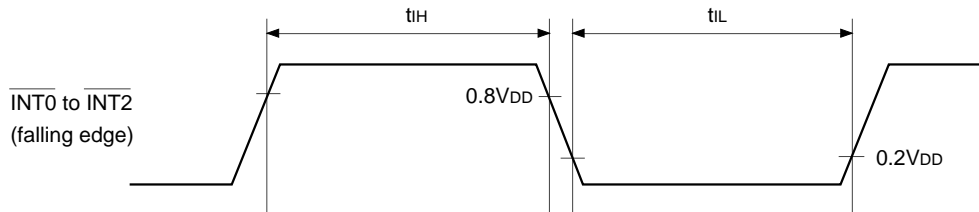


**(3) Interrupt, Reset input**

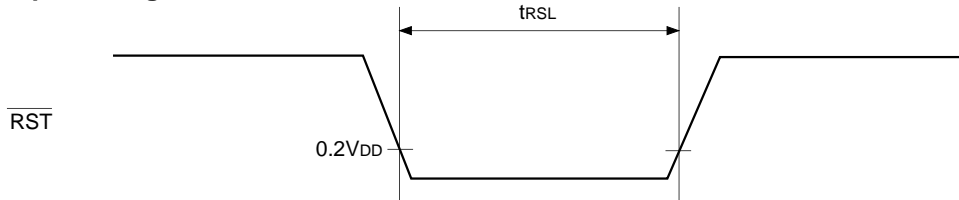
( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt high and low level widths	$t_{IH}$ $t_{IL}$	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$		1		$\mu\text{s}$
Reset input low level width	$t_{RSL}$	$\overline{\text{RST}}$		$8/f_c$		$\mu\text{s}$

**Fig. 5. Interrupt input timing**



**Fig. 6.  $\overline{\text{RST}}$  input timing**



**(4) Power-on reset**

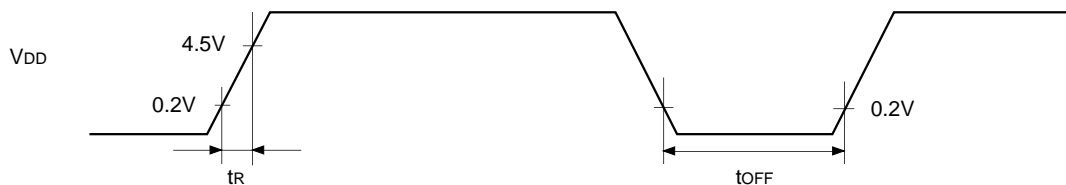
**Power-on reset\***

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	$t_R$	$V_{DD}$	Power-on reset	0.05	50	ms
Power supply cut-off time	$t_{OFF}$		Repetitive power-on	1		ms

\* Specifies only when power-on reset function is selected.

**Fig. 7. Power-on reset**



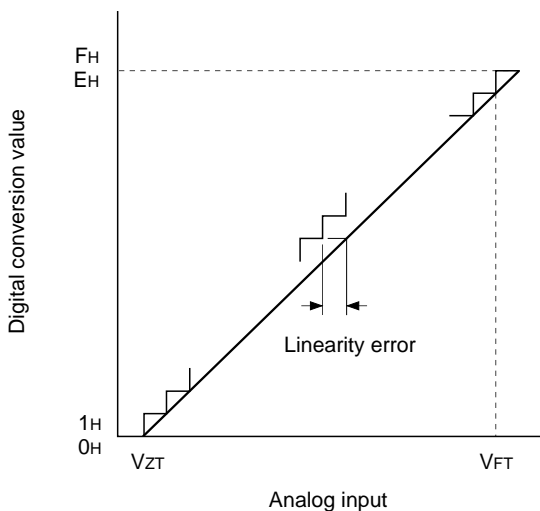
The power supply should rise smoothly.

(5) A/D converter characteristics

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						4	Bits
Linearity error			Ta = 25°C VDD = 5.0V VSS = 0V			±1	LSB
Zero transition voltage	VZT*1			-10	160	320	mV
Full-scale transition voltage	VFT*2			4370	4530	4690	mV
Conversion time	tCONV			160/fc			µs
Sampling time	tSAMP			12/fc			µs
Analog Input voltage	VIAN	AN0 to AN3		0		VDD	V

Fig. 8. Definitions for A/D converter terms



\*1) VZT: Indicates the value that digital conversion value changes from 00H to 01H and vice versa.

\*2) VFT: Indicates the value that digital conversion value changes from EH to FH and vice versa.

**Note)** For 4-bit conversion, correction of the upper 5 bits A/D data register (ADD: address 00F5H) into 4 bit data is defined according to the following program example.

(A/D converter program example)

```

MOV    A, ADD      ; ACC ← conversion data
LSR    A           ; logical shift right (4 times)
LSR    A           ;
LSR    A           ;
LSR    A           ;
ADC    A, #00H     ; carry addition (if AD3 is 1, data is incremented)
CMP    A, #10H     ;
BNE    ADC_SKIP   ;
MOV    A, #0FH     ;
    
```

ADC\_SKIP:

(6) I<sup>2</sup>C bus timing

(T<sub>a</sub> = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock high level width	t <sub>HIGH</sub>	SCL		4.0		μs
Set-up time for repetitive transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*		μs
Data set-up time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Set-up time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\* Since SCL rise time (max: 300ns) is not considered part of data hold time, allow at least 300ns.

Fig. 9. I<sup>2</sup>C Bus transfer data timing

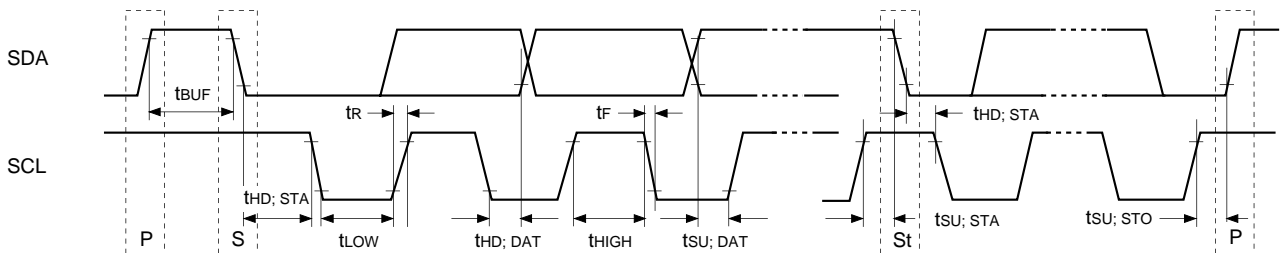
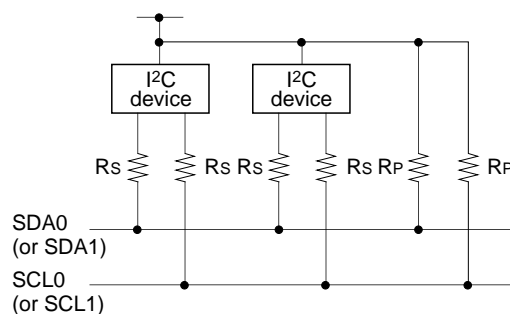


Fig. 10. I<sup>2</sup>C device recommended circuit

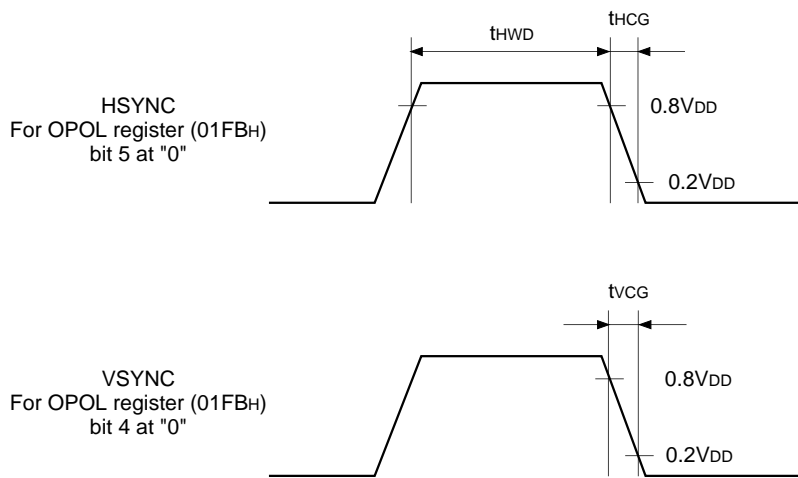


- A pull-up resistor must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (R<sub>S</sub> = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

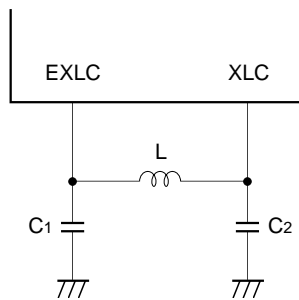
**(7) OSD (On Screen Display) timing** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
OSD clock frequency	fosc	EXLC XLC	Fig. 12	4	13	MHz
HSYNC pulse width	tHWD	HSYNC	Fig. 11	1.2		μs
HSYNC afterwrite rise and fall times	tHCG	HSYNC	Fig. 11		200	ns
VSYNC afterwrite rise and fall times	tVCG	VSYNC	Fig. 11		1.0	μs

**Fig. 11. OSD timing**



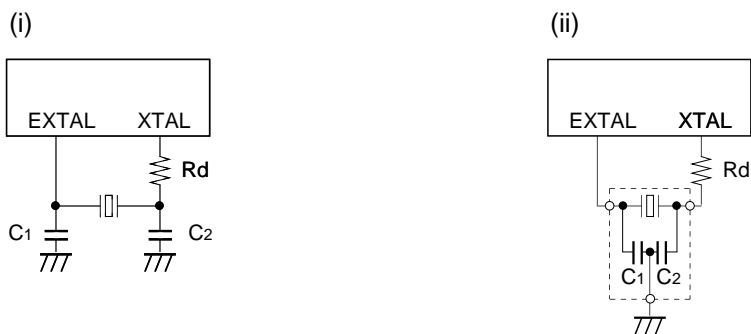
**Fig. 12. LC oscillator circuit connection**





Supplement

Fig. 13. Recommended Oscillation Circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
RIVER ELETEC CO., LTD.	HC-49/U03	4.00	15	15	0	(i)
		4.19				
KINSEKI LTD.	HC49/U (-S)	4.00	22	22	0	
		4.19	18	18		

\* Indicates types with on-chip grounding capacitors (C1 and C2).

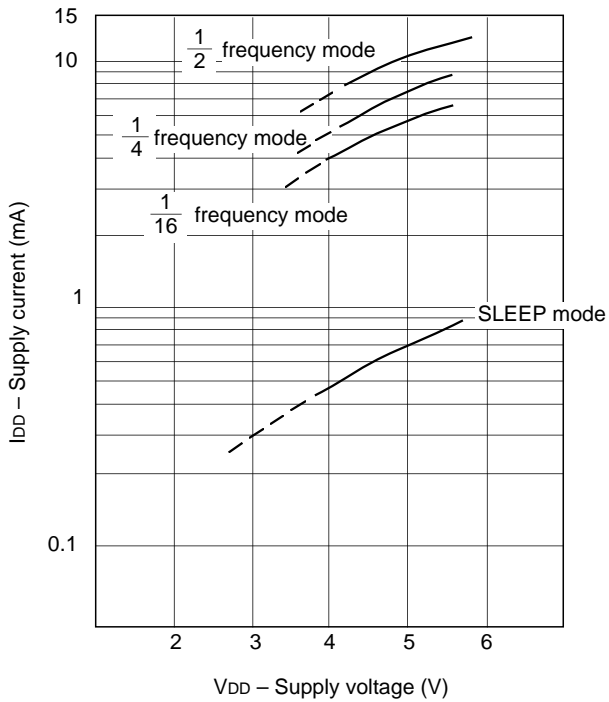
Selection Guide

Option item	Mask version	CXP851P16AS-1-□□□	CXP851P16AQ-1-□□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP	64-pin plastic QFP
PROM capacitance	12K/16K bytes	PROM 16K bytes	PROM 16K bytes
Reset pin pull-up resistor	Existent/non-existent	Existent	Existent
Power-on reset circuit	Existent/non-existent	Existent	Existent
Font data	User specified	User specified (PROM) *	User specified (PROM) *

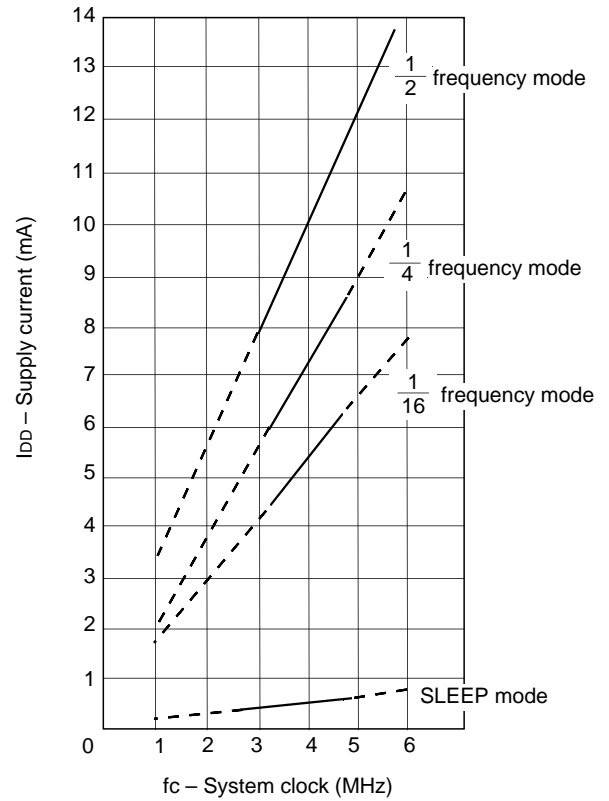
\* The font data for the one-time PROM version is operated in the same way as the program writing.

Fig. 14. Characteristic curves

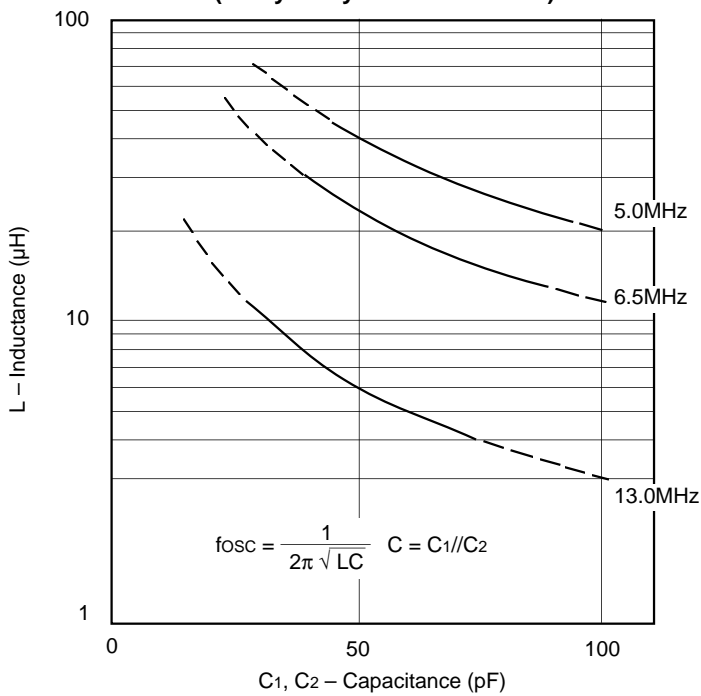
**I<sub>DD</sub> vs. V<sub>DD</sub> (f<sub>c</sub> = 4MHz, T<sub>a</sub> = 25°C, Typical)**



**I<sub>DD</sub> vs. f<sub>c</sub> (V<sub>DD</sub> = 5V, T<sub>a</sub> = 25°C, Typical)**



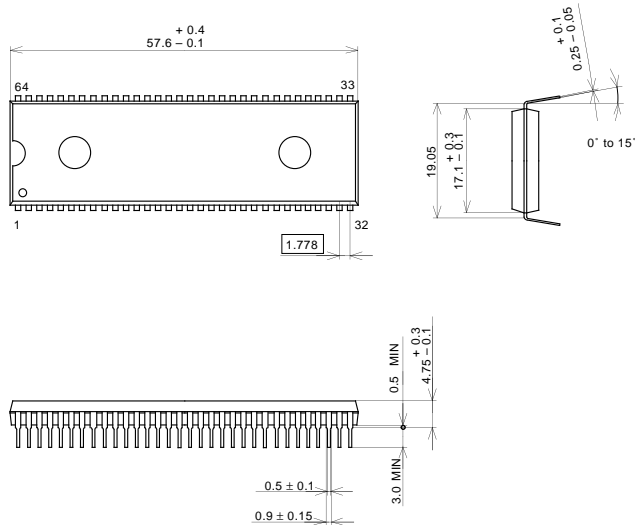
**Parameter Curve for OSD Oscillator L vs. C (Analytically calculated value)**



Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

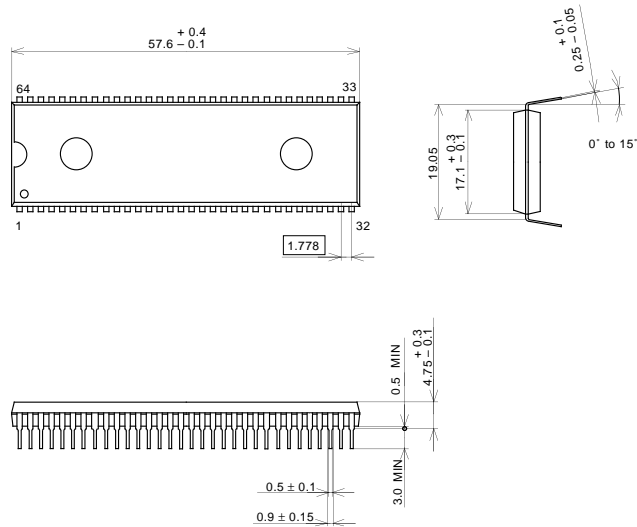


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

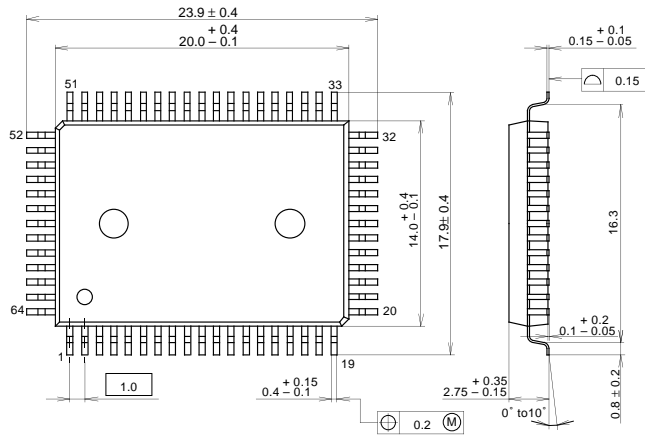
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m

Package Outline Unit: mm

64PIN QFP (PLASTIC)

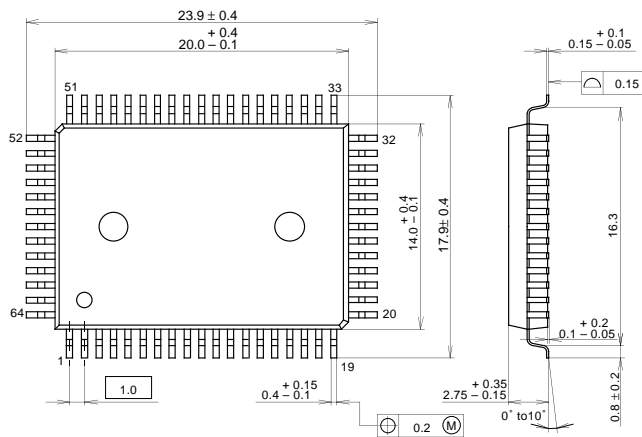


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m